

Institute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 1207.P006D	Application Number: 10/021,744
	First Named Inventor: Ting et al.	
	Filing Date: December 5, 2001	

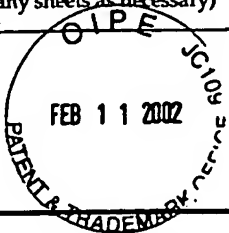
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### U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (If known)			
		4,020,469		Manning Technology Center	2109-26-77	
		4,661,901		Veneski	4-28-87	
		4,700,187		Furtek	10-13-87	
		4,720,780		Dolecek	1-19-88	
		4,736,333		Mead et al.	4-5-88	
		4,815,003		Putatunda et al.	3-21-89	
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Exam. Initial*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (If known)				
		EP	0415542 A1	A1	Advanced Micro Devices, Inc.	03/06/91		
		EP	0630115 A2	A2	Pilkington Micro-Electronics Limited	12/21/94		
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		GB	2295738 A		Altera Corporation	06/05/96		

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		5,243,238		Kean	9-7-93	
		5,260,610		Pedersen et al.	11-9-93	
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		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (If known)				
		PCT	WO92/08286	A1	Concurrent Logic, Inc.	05/14/92		
		PCT	WO94/28475	A1	Regents of the University of California	12/08/94		
		PCT	WO96/05964	A1	Minnesota Mining and Manufacturing Company	02/29/96		
		PCT	WO96/35261	A1	BTR, Inc.	11/07/96		

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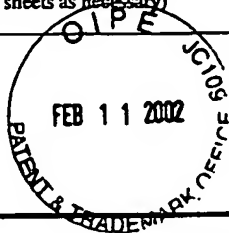
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Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
e		RICHARD CLIFF et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.3.1-7.3.5.	
		Altera Corporation, Data Sheet, "Flex EPF81188 12,000-Gate Programmable Logic Device", September 1992, Version 1.	
		MINNICK, R.C., "A Survey of Microcellular Research", Journal of the Association for Computing Machinery, Vol. 14, No. 2, April 1967, pp. 203-241.	
		SHOUP, R.G., "Programmable Cellular Logic Arrays", Ph.D dissertation, Carnegie-Mellon University, Pittsburgh, PA, March 1970 - Partial.	
		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits", UNIVAC, Division of Sperry Rand Corporation, Blue Bell, PA, Contract AF 19 (628)2907, AFCRL 66-298, Project No. 464504, November 30, 1965.	
		PING-TSUNG WANG et al., "A High Performance FPGA with Hierarchical Interconnection Structure", Institute of Electrical and Electronic Engineers, pp. 239-242, May 30, 1994.	
		Motorola Product Brief, "MPA10XX Field Programmable Gate Arrays", pp. 4 pages total, September 27, 1993.	
		KRAMBECK, R.H. "ORCA: A High Performance, Easy to Use SRAM Based Architecture", Wescon '93 record, pp. 310-320, September 20-30, 1993.	
		BUFFOLI et al., "Dynamically Reconfigurable Devices used to Implement a Self-Tuning, High Performance PID Controller », IEEE 1989, pp. 107-112.	
		DEVADAS, S., "Boolean Decomposition of Programmable Logic Arrays", IEEE 1988, pp. 2.5.1-2.5.5.	
		VIDAL, J., "Implementing Neural Nets with Programmable Logic", IEEE 1988, pp. 50-53.	

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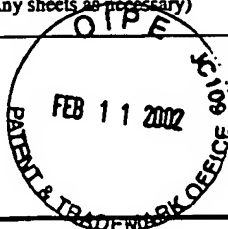
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		YACHYANG SUN et al., "An Area Minimizer for Floorplans with L-Shaped Regions", 1992, Int'l. Conference on Computer Design, pp. 383-386.	
		ATMEL Corporation, "Field Programmable Gate Arrays - AT6000 Series", 1993.	
		DAVE BURSKY, "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy", Electronic Design, pp. 33-34, October 1, 1993.	
		DICK L. LIU et al., "Design of Large Embedded CMOS PLA's for Built-In Self-Test", IEEE 1988, pp. 50-53.	
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		BARRY K. BRITTON et al., "Optimized Reconfigurable Cell Array Architecture for High Performance Field Programmable Gate Arrays", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.2.1-7.2.5.	
		TING et al., "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", pp. 1-10.	
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